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APPLICATION

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TITLE: ARCHITECTURE FOR ADVANCED SERIAL LINK BETWEEN TWO CARDS

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ARCHITECTURE FOR ADVANCED SERIAL LINK BETWEEN TWO CARDS

RELATED APPLICATIONS

This application claims the benefits of provisional patent application Serial No. 60/262,358, filed January 16, 2001, for "Global Architecture for Advanced Serial Link" (Docket No. RAL920010004US1).

This application is related to the following copending applications, all of which are incorporated herein by reference: Serial No. _____, filed _____, for "Unified Digital Architecture" (Docket No. RAL920010003US2); Serial No. _____, filed _____, for "Analog Unidirectional Serial Link Architecture" (Docket No. RAL920010005US2) ; and Serial No._____ , filed_____, for "Apparatus And Method For Oversampling With Evenly Spaced Samples" (Attorney Docket No. RAL920010011US2).

FOSTER-FREEMAN

FIELD OF THE INVENTION

This invention relates generally to the transfer of data in serial form from a register on one ASIC (application specific integrated circuit) chip on a card to a register on another ASIC chip on a card and, more particularly, to the serial transfer of such data wherein the data is converted from parallel digital form to serial analog form for transfer from one ASIC to the second ASIC and is then reconverted to parallel digital form in the second ASIC, after it has been transferred, in serial analog form.

BACKGROUND OF THE INVENTION

Serial data must be transmitted across wired media. The transmit and receive sections include chips wired to one another and card-to-card interconnects. The

transmission media can be a combination of printed circuit boards, connectors, back plane wiring, fiber or cable. The interconnect can include its own power, data and clocking sources or may derive these functions from a host module. Such data has typically been transmitted through a parallel data bus, such as ISA, PCI, PCI-X and the like. One drawback of such parallel links is the moderate rate of data transmission due to improved microprocessor performance, resulting in data transfer bandwidths that typically outpace I/O transfer rates. Also, the ASIC I/O count is high. In addition, the system integration I/O count using a parallel data bus is high. Finally, the overall system cost associated with the use of the parallel data bus tends to be high.

Related art shows attempts to overcome these difficulties and drawbacks by utilizing serial communication systems involving a variety of schemes. For example, some have used a carrierless amplitude/phase (CAP) modulation scheme. Others have used linear compression/decompression and digital signal processing techniques for frequency modulation. Still others use a linear (analog) phase rotator to recover only the carrier of an incoming signal. Some transmit using a pass band which limits the bandwidth of the frequencies being passed, rather than a baseband channel wherein the signals are not shared and the frequencies are not restricted.

SUMMARY OF THE INVENTION

The present invention comprises a global architecture for a serial link connection between two cards which must transmit data across wired media. The architecture comprises a transmitter and a receiver. The transmitter includes circuitry and a structure to take digital bits from a bit register, such as for example, an eight-bit register or a ten-bit

register, and convert these bits into serial analog transmission to the receiver. The receiver includes a structure and circuitry to sample edges of the data on analog transmission of the original digital bits and reconvert the analog serial signal of the digital bits to the original digital bits and store them in a register comparable to the data stored in the original register from which they were selected.

DESCRIPTION OF THE DRAWINGS

Figure 1 is a high level diagram showing the wired interconnection between the transmitter portion and the receiver portion of the serial link;

Figure 2 is a block diagram showing the operation of the circuitry of the transmitter of the architecture; and

Figure 3 is a block diagram showing the operation of the circuitry of the receiver of the architecture.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawings and, for the present, to Figure 1, a high level diagram of interconnection of ASICs showing a transmitter on one side of the connection and a receiver on the other side of the connection for several different transmitter and receivers for passing information is shown. The present invention, as indicated above, can be implemented in any one of several different configurations, such as a combination of a printed circuit boards, connectors, back plane wiring, fiber or cable. As shown, the implementation will be on a back plane with hard wiring between the transmitting portion and the receiving portion.

As can be seen in Figure 1, a back plane 10 is provided which has mounted thereon a pair of printed circuit (PC) cards 12a and 12b. Each circuit card 12a and 12b is provided with, respectively, ASIC chips 14a and 14b which are to be interconnected according to the present invention. Each ASIC 14a, 14b has at least one transmitter 16 and, as illustrated, has two such transmitters, although more can be provided. Also, each ASIC 14a, 14b is provided with at least one receiver 18; again, the illustrated embodiment shows two receivers 18, although, as indicated above with respect to the transmitter 16, more than two can be provided. Generally speaking, the transmitter 16 and receiver 18 are provided in pairs since data generally will have to flow in both directions and the connection described herein is unidirectional. Each transmitter 16 on ASIC 14a or 14b includes one-way hard wired serial buses 20 interconnecting the transmitter 16 on one ASIC 14a or 14b to a receiver 18 on the other ASIC 14a or 14b. Thus, two-way communication is provided by having paired transmitters and receivers on each ASIC 14a or 14b.

Briefly, each transmitter 16 has stored therein parallel digital data in a register 24 (Fig. 2). The transmitter 16 converts this stored, parallel, digital data in the register 24 in one ASIC, eg. 14a, to serial analog form, transmits the data in serial analog form on one of the serial buses 20 to the receiver 18 associated therewith on the opposite ASIC, eg. 14b. The receiver 18 converts the analog asynchronous serial data to synchronous, parallel, digital data for storage 68 (Figure 3) in a register in digital form.

Thus, the function of the serial link herein is to take parallel data in a register in an efficient manner, transmit it in an asynchronous serial analog form and reconvert it to synchronous, parallel, digital data.

Referring now to Figure 2, a block diagram of the circuitry function of a transmitter 16 is shown. As can be seen, the transmitter 16 includes a bit register 24. Typically, this is either an eight-bit or a ten-bit register, although other size registers could be used. The description of this particular register 24 will be as a ten-bit register. A two-bit of ten bit selector 26 is provided which will select two bits at a time sequentially from the register 24. This is done under the synchronous control of counter 38. It is to be understood that other than two bits at a time can be read from the register 24. However, this number must be a number that is evenly divisible into the number of bits in the register 24. Thus, in the case of a ten-bit register, this could be one, two or five and, in the case of an eight-bit register, this could be one, two or four. Two bits are preferred.

Each of the two bits selected by the selector 26 from the register 24 is provided to a bit latch 28a or 28b. This selection and delivery is also under the synchronous control of counter 38. The bits are then delivered from the latches 28a and 28b to a multiplexor 30, also under the synchronous control of counter 38, and then to a one-bit latch 32. From the one-bit latch 32, the bits are delivered to a driver equalizer 34, which will convert the received digital bits from the latch 32 to a serial analog signal output 35 containing the converted digital bits.

A single phase, full rate, phase lock loop 36 is provided which will clock the action of the latch 32 and driver equalizer 34, and also will actuate the counter 38 which, in turn, has inputs to the multiplexor 30, the latches 28a and 28b, the select 26 and the ten-bit register 24. The phase lock loop 36 has as an input thereto a clock signal, which can be internal or external from clock 40, as shown. The counter 38 functions to provide

synchronous operation of the extraction of the bits from the register 24 by the selector 26 for delivery to the latches 28a and 28b. Also, the counter operates to form a synchronous delivery of the bits from the latches 28a and 28b to the multiplexor 30 and therefrom to the latch 32. It is at the driver equalizer 34 that the digital bits synchronously received are converted to a serial analog signal 35. The functioning and more detailed description of the various parts of the transmitter 16, such as the bit register 24, selector 26, the latches 28a and 28b, the multiplexor 30, the latch 32, the single phase, full rate, phase lock loop 36 and the counter 38 are all described in more detail in application Serial No. _____, filed _____, for "Unified Digital Architecture" (Docket No. RAL920010003US2) and application Serial No._____, filed _____, for "Analog Unidirectional Serial Link Architecture" (Docket No. RAL920010005US2), which applications are incorporated herein by reference. The analog output 35 is placed on the serial bus 20. It is transmitted in an asynchronous form to the receiver 18 attached to the other end of the serial bus 20. As indicated above, the receiver 18 receives the asynchronous analog signal and converts it to a synchronous digital parallel signal corresponding to the digital bits in register 24 for storage in the receiver 18.

Referring now to Figure 3, a block diagram showing the structure and circuitry function for converting the asynchronous analog serial signal 35 to a synchronous digital parallel digital bits for storage in the receiver 18 for storing bits is shown. The serial analog asynchronous signal 35 is received by a signal receiving member 50 which delivers the analog signal to sample latches 52. In the sample latches 52, the analog signal is converted to a digital signal by means of a phase rotator 54 which operates under the control of a data

detection and edge detection circuit 58 and a multi-phase, half rate phase loop lock 60. This technique operates by sampling, and preferably multiple sampling, both edges of the data in the analog signal and converts the data in the analog signal to parallel data bits. Preferably, the multiple samples are used to determine the approximate center point of each resulting data bit. This is an oversampling circuit which will convert the asynchronous analog serial signal in selector 62 to a digital output 63 in two-bit increments delivered to a shift register 64. A counter 66, which is actuated by the phase rotator 54, operates on shift register 64 to output the two-bit digital signals as ten-bit synchronous signals to ten-bit register 68. The operation of this receiver 18 is described in detail in application Serial No._____, filed _____, for "Analog Unidirectional Serial Link Architecture" (Docket No. RAL920010005US2), and application Serial No. _____, filed _____, for "Apparatus and Method for Oversampling with Evenly Spaced Samples" (Docket No. RAL920010011US2), which applications are incorporated herein by reference.

Thus, the ten-bit digital bits stored as parallel data in the ten-bit register 24 are converted by the transmitter 16 to an asynchronous analog serial signal 35 which is to be transported asynchronously on bus 20, which asynchronous analog signal 35 is then reconstituted by the receiver 18 to the original ten-bit parallel digital bit in register 68.

While the invention has been described in combination with embodiments thereof, it is evident that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the foregoing teachings. Accordingly, the invention

is intended to embrace all such alternatives, modifications and variations as fall within the spirit and scope of the appended claims.

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